

Class	Subclass	ISSUE CLASSIFICATION
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PATENT NUMBER

**U.S. UTILITY Patent Application**

HKM O.I.P.E. PD SCANNED Q.A. Am	PATENT DATE
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APPLICATION NO. 09/747703	CONT/PRIOR	CLASS 34 <del>430</del>	SUBCLASS 006	ART UNIT <del>28</del> F146	EXAMINER: KORNAKOV MAROFF
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## APPLICANT'S

Thomas Nguyen

**37**

## Method and apparatus for reducing the backside faults during wafer processing

PTO-2040  
12/89

<b>ISSUING CLASSIFICATION</b>									
<b>ORIGINAL</b>		<b>CROSS REFERENCE(S)</b>							
<b>CLASS</b>	<b>SUBCLASS</b>	<b>CLASS</b>	<b>SUBCLASS (ONE SUBCLASS PER BLOCK)</b>						
<b>INTERNATIONAL CLASSIFICATION</b>									

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<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)           _____ (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner)           _____ (Date)			<b>ISSUE FEE</b>	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)           _____ (Date)			<b>ISSUE BATCH NUMBER</b>	

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